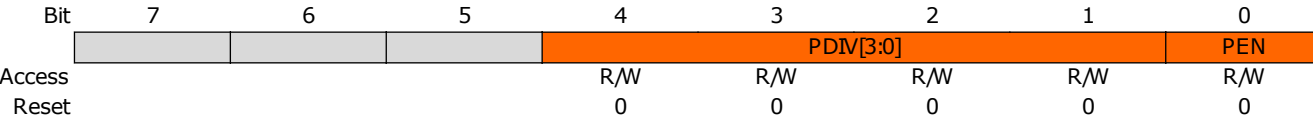

Bits 4:1 – PDIV[3:0] Prescaler Division

This bit field controls the division ratio of the Main Clock (CLK_MAIN) prescaler, when the Prescaler (PEN) bit is '1'.

Value	Name	Description
0x0	2X	Divide by 2
0x1	4X	Divide by 4
0x2	8X	Divide by 8
0x3	16X	Divide by 16
0x4	32X	Divide by 32
0x5	64X	Divide by 64
0x8	6X	Divide by 6
0x9	10X	Divide by 10
0xA	12X	Divide by 12
0xB	24X	Divide by 24
0xC	48X	Divide by 48
Other	-	Reserved

Note: Configuration of the input frequency (CLK_MAIN) and prescaler settings must not exceed the allowed maximum frequency of the peripheral clock (CLK_PER) or CPU clock (CLK_CPU). Refer to the *Electrical Characteristics* section for further information.

Bit 0 – PEN Prescaler Enable

This bit controls whether the Main Clock (CLK_MAIN) prescaler is enabled or not.

Value	Description
0	The CLK_MAIN prescaler is disabled
1	The CLK_MAIN prescaler is enabled, and the division ratio is controlled by the Prescaler Division (PDIV) bit field