

|        |         |   |   |   |   |   |   |     |
|--------|---------|---|---|---|---|---|---|-----|
| Bit    | 7       | 6 | 5 | 4 | 3 | 2 | 1 | 0   |
|        | INTTYPE |   |   |   |   |   |   | CFD |
| Access | R/W     |   |   |   |   |   |   | R/W |
| Reset  | 0       |   |   |   |   |   |   | 0   |

### Bit 7 – INTTYPE Interrupt Type

This bit controls the type of the Clock Failure Detection (CFD) interrupt.

| Value | Name | Description            |
|-------|------|------------------------|
| 0     | INT  | Regular Interrupt      |
| 1     | NMI  | Non-Maskable Interrupt |

**Note:** This bit is read-only when the Clock Failure Detection Enable (CFDEN) bit in the Main Clock Control C (CLKCTRL.MCLKCTRLC) register is '1', and both the Clock Failure Detection (CFD) interrupt enable bit and this bit are '1.' This bit will remain read-only until a System Reset occurs.

### Bit 0 – CFD Clock Failure Detection Interrupt Enable

This bit controls whether the Clock Failure Detection (CFD) interrupt is enabled or not.

| Value | Description                   |
|-------|-------------------------------|
| 0     | The CFD interrupt is disabled |
| 1     | The CFD interrupt is enabled  |

**Note:** This bit is read-only when the Clock Failure Detection Enable (CFDEN) bit in the Main Clock Control C (CLKCTRL.MCLKCTRLC) register is '1', and both the Interrupt Type (INTTYPE) bit and this bit are '1.' This bit will remain read-only until a System Reset occurs.