| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | RUNSTDBY | | CSUTHF[1:0] | | FRQRANGE[1:0] | | SELHF | ENABLE |
| Access | R/W | | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | | 0 | 0 | 0 | 0 | 0 | 0 |

**Bit 7 – RUNSTDBY** Run Standby
This bit controls whether the External High-Frequency Oscillator (XOSCHF) is always running or not, when the ENABLE bit is '1'.

| Value | Description |
|---|---|
| 0 | The XOSCHF oscillator will only run when requested by a peripheral or by the main clock (1) |
| 1 | The XOSCHF oscillator will always run in Active, Idle and Standby sleep modes (2) |

**Notes:**

1. The requesting peripheral, or the main clock, must take the oscillator start-up time into account.
2. The oscillator signal is only available if requested, and will be available after two XOSCHF cycles, if the initial crystal start-up time has already ended.

**Bits 5:4 – CSUTHF[1:0]** Crystal Start-up Time
This bit field controls the start-up time for the External High-Frequency Oscillator (XOSCHF), when the Source Select (SELHF) bit is '0'.

| Value | Name | Description |
|---|---|---|
| 0x0 | 256 | 256 XOSCHF cycles |
| 0x1 | 1K | 1K XOSCHF cycles |
| 0x2 | 4K | 4K XOSCHF cycles |
| 0x3 | - | Reserved |

**Note:** This bit field is read-only when the ENABLE bit or the External Crystal/Clock Status (XOSCHFS) bit in the Main Clock Status (MCLKSTATUS) register is '1'.

**Bits 3:2 – FRQRANGE[1:0]** Frequency Range
This bit field controls the maximum frequency supported for the external crystal. The larger the range selected, the higher the current consumption by the oscillator.

| Value | Name | Description |
|---|---|---|
| 0x0 | 8M | Max. 8 MHz XTAL frequency |
| 0x1 | 16M | Max. 16 MHz XTAL frequency |
| 0x2 | 24M | Max. 24 MHz XTAL frequency |
| 0x3 | 32M | Max. 32 MHz XTAL frequency |

**Note:** If a crystal with a frequency larger than the maximum supported CLK_CPU frequency is used and used as the main clock, it is necessary to divide it down by writing the appropriate configuration to the PDIV bit field in the Main Clock Control B register.

**Bit 1 – SELHF** Source Select
This bit controls the source of the External High-Frequency Oscillator (XOSCHF).

| Value | Name | Description |
|---|---|---|
| 0 | CRYSTAL | External Crystal on the XTALHF1 and XTALHF2 pins |
| 1 | EXTCLOCK | External Clock on the XTALHF1 pin |

**Note:** This bit field is read-only when the ENABLE bit or the External Crystal/Clock Status (XOSCHFS) bit in the Main Clock Status (MCLKSTATUS) register is '1'.

**Bit 0 – ENABLE** Enable
This bit controls whether the External High-Frequency Oscillator (XOSCHF) is enabled or not.

| Value | Description |
|---|---|
| 0 | The XOSCHF oscillator is disabled |
| 1 | The XOSCHF oscillator is enabled, and overrides normal port operation for the respective oscillator pins |