

BANK 56		BANK 57		BANK 58		BANK 59		BANK 60		BANK 61		BANK 62		BANK 63					
1C00h	Core Registers	1C80h	Core Registers	1D00h	Core Registers	1D80h	Core Registers	1E00h	Core Registers	1E80h	Core Registers	1F00h	Core Registers	1F80h	Core Registers				
1C0Bh	Unimplemented Read as '0'	1C8Bh	Unimplemented Read as '0'	1D0Bh	Unimplemented Read as '0'	1D8Bh	Unimplemented Read as '0'	1E0Bh	See Table 2 for register mapping details	1E8Bh	See Table 3 for register mapping details	1F0Bh	Unimplemented Read as '0'	1F8Bh	Unimplemented Read as '0'				
1C0Ch		1C8Ch		NVMADRL		1D0Ch		ADLTHL		1D8Ch		RA0PPS		1E0Ch		1E8Ch	1F0Ch	UMTOAP	1F8Ch
		1C8Dh		NVMADRH		1D0Dh		ADLTHH		1D8Dh		RA1PPS					1F0Dh	UMTOAL	
		1C8Eh		NVMDATL		1D0Eh		ADUTHL		1D8Eh		RA2PPS					1F0Eh	UMTOAH	
		1C8Fh		NVMDATH		1D0Fh		ADUTHH		1D8Fh		—					1F0Fh		
		1C90h		NVMCON1		1D10h		ADERRL		1D90h		RA4PPS							
		1C91h		NVMCON2		1D11h		ADERRH		1D91h		RA5PPS							
		1C92h		SCANCON0		1D12h		ADSTPTL		1D92h		Unimplemented Read as '0'							
		1C93h		SCANLADRL		1D13h		ADSTPTH											
		1C94h		SCANLADRH		1D14h		ADFLTRL		1D97h									
		1C95h		—		1D15h		ADFLTRH		1D98h		RB4PPS ⁽¹⁾							
		1C96h		SCANHADRL		1D16h		ADACCL		1D99h		RB5PPS ⁽¹⁾							
		1C97h		SCANHADRH		1D17h		ADACCH		1D9Ah		RB6PPS ⁽¹⁾							
		1C98h		—		1D18h		ADACCU		1D9Bh		RB7PPS ⁽¹⁾							
		1C99h		SCANDPS		1D19h		ADCNT		1D9Ch		RC0PPS							
		1C9Ah		SCANTRIG		1D1Ah		ADRPT		1D9Dh		RC1PPS							
		1C9Bh		—		1D1Bh		ADPREVL		1D9Eh		RC2PPS							
		1C9Ch		—		1D1Ch		ADPREVH		1D9Fh		RC3PPS							
		1C9Dh		CRCDATA1		1D1Dh		ADRESL		1DA0h		RC4PPS							
		1C9Eh		CRCDATAH		1D1Eh		ADRESH		1DA1h		RC5PPS							
		1C9Fh		CRCDATAU		1D1Fh		ADPCH		1DA2h		RC6PPS ⁽¹⁾							
		1CA0h		CRCDATAT		1D20h		—		1DA3h		RC7PPS ⁽¹⁾							
		1CA1h		CRCOUTL		1D21h		ADACQL		1DA4h		Unimplemented Read as '0'							
		1CA2h		CRCOUTH		1D22h		ADACQH		1DBFh									
		1CA3h		CRCOUTU		1D23h		ADCAP		1DC0h		TRISA0PPS							
		1CA4h		CRCOUTT		1D24h		ADPREL		1DC1h		TRISA1PPS							
		1CA5h		CRCCON0		1D25h		ADPREH		1DC2h		TRISA2PPS							
	1CA6h	CRCCON1	1D26h	ADCON0	1DC3h	—													
	1CA7h	CRCCON2	1D27h	ADCON1	1DC4h	TRISA4PPS													
	1CA8h	Unimplemented Read as '0'	1D28h	ADCON2	1DC5h	TRISA5PPS													
			1D29h	ADCON3	1DC6h	Unimplemented Read as '0'													
			1D2Ah	ADSTAT															
			1D2Bh	ADREF															
			1D2Ch	ADACT															
			1D2Dh	ADCLK															
			1D2Eh	ADCG1A															
			1D2Fh	ADCG1B ⁽¹⁾															
			1D30h	ADCG1C															
			1D31h	Unimplemented Read as '0'															
1C6Fh	Common RAM (Accesses 70h-7Fh)	1CEFh	Common RAM (Accesses 70h-7Fh)	1D6Fh	Common RAM (Accesses 70h-7Fh)		1DEFh	Common RAM (Accesses 70h-7Fh)	1E6Fh	Common RAM (Accesses 70h-7Fh)	1EEFh	Common RAM (Accesses 70h-7Fh)	1F6Fh	Common RAM (Accesses 70h-7Fh)	1FEFh	Common RAM (Accesses 70h-7Fh)			
1C70h		1CF0h		1D70h		1DF0h	1E70h		1EF0h		1F70h								
1C7Fh		1CFh		1D7Fh		1DFh	1E7Fh		1EFh		1F7Fh								
												1FE3h							
												1FE4h			STATUS_SHAD				
												1FE5h			WREG_SHAD				
												1FE6h			BSR_SHAD				
												1FE7h			PCLATH_SHAD				
												1FE8h			FSROL_SHAD				
												1FE9h			FSROH_SHAD				
												1FEAh			FSR1L_SHAD				
												1FEBh			FSR1H_SHAD				
												1FECh			—				
												1FEDh			STKPTR				
												1FEEh			TOSL				
												1FEFh			TOSH				

Note: 1. Available on 20-pin devices only

Legend:

■ Unimplemented data memory locations, read as '0'