ON[(1)]

RUN[(2)]

TUCLK

Fosc/4

TUxyTMR 0[(3)] 1 2 3 4 = PR 0 1

TUxyCR 2 1

CAPT

ERS

PR Match
TMR = PR

Timer Out
(Pulse)

Timer Out
(Level)

ZIF (4)

PRIF (4)

CIF (4) (4)

Timer Setup:

START = None (ON = 1) RESET = At PR Match STOP = Rising ERS Edge
CSYNC = Async OSEN = Enabled
PR = 4 (Period of 5) PS = 2 (Prescaler of 3)

Note:

1. The ON bit is set in the software and cleared by hardware upon Stop (One Shot mode).
2. The RUN trace illustrates the actual RUN SFR bit and not the internal Timer Clock domain run/stop signal.
3. Ensure that TUxyTMR counter is reset to zero by setting CLR command.
4. Cleared by software.