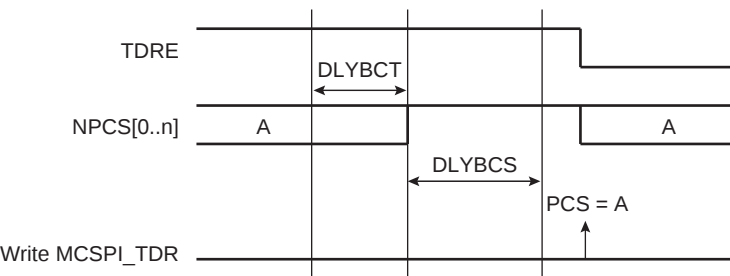
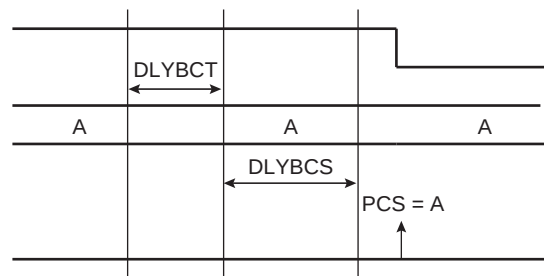


CSAAT = 0 and CSNAAT = 0



CSAAT = 1 and CSNAAT= 0 / 1

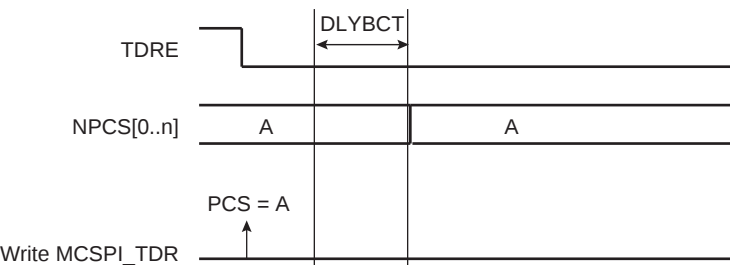


Timing diagram showing the relationship between NPCS[0..n] and TDRE signals. The diagram illustrates the delay between the NPCS[0..n] signal and the TDRE signal, labeled as DLYBCT (NPCS[0..n] delay before chip select turn-off). The NPCS[0..n] signal is shown as a pulse, and the TDRE signal is shown as a pulse. The delay DLYBCT is indicated by a double-headed arrow between the falling edge of NPCS[0..n] and the falling edge of TDRE.

Timing diagram showing the relationship between NPCS[0..n] and TDRE signals. The diagram illustrates the delay between the command (NPCS[0..n]) and the start of the transfer (TDRE). Key parameters shown are DLYBCT (Delay Between Command and Transfer) and DLYBCS (Delay Between Command and Start). The PCS = B period is also indicated, starting from the Write MCSPI_TDR signal.

Timing diagram for PCS = B. The diagram shows two signals, A and B, over time. Signal A is high for a duration DLYBCT before signal B becomes high. The delay DLYBCT is labeled with a double-headed arrow. The delay DLYBCS is labeled with a double-headed arrow. The signal B is labeled PCS = B.

CSAAT = 0 and CSNAAT = 0



CSAAT = 0 and CSNAAT = 1

