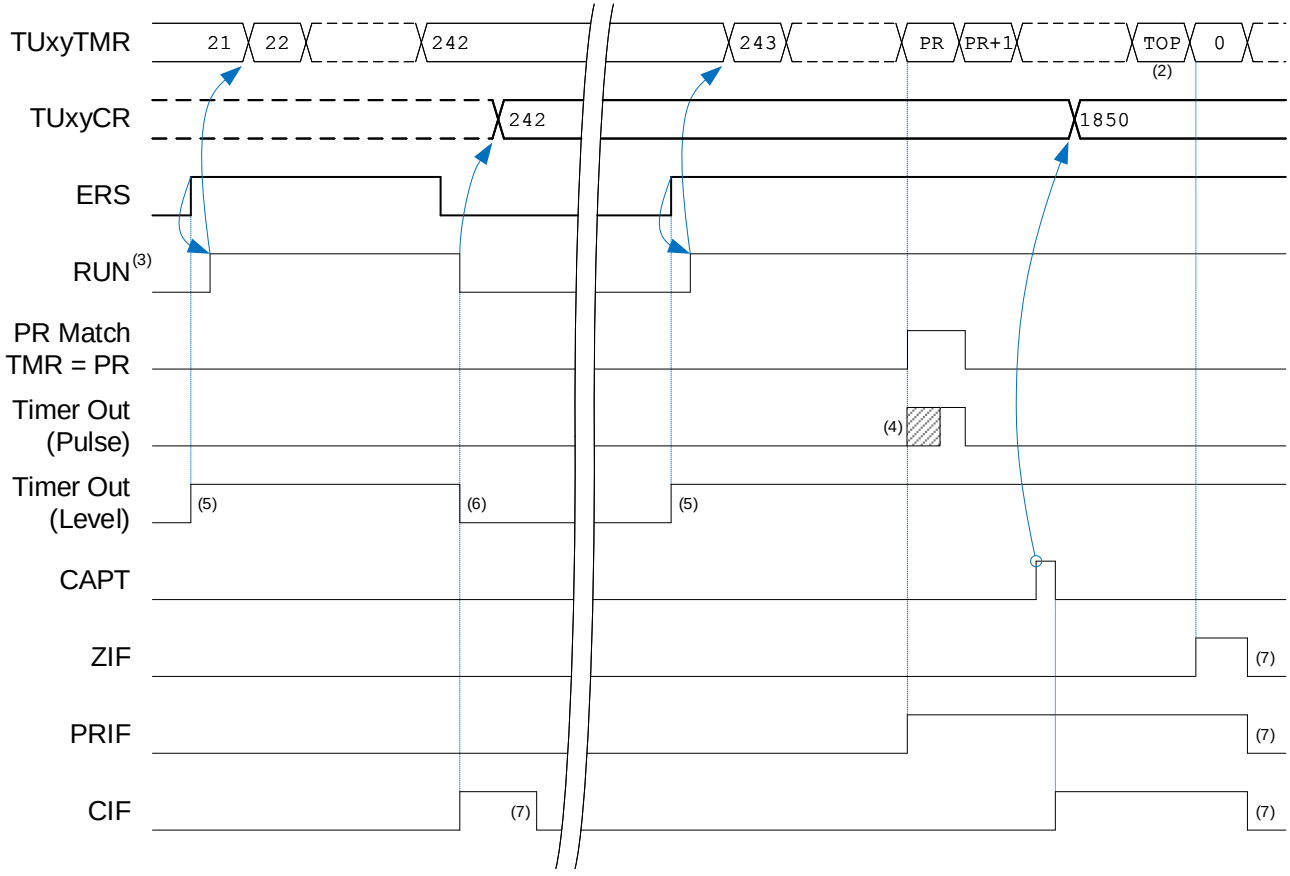

Timer Setup:

START = Rising ERS Edge RESET = None STOP = Either ERS Edge
CSYNC = Sync

Note:

1. Cross-domain clock synchronization applies as required but is not highlighted.
2. `TOP` represents the maximum counter value.
3. The RUN trace illustrates the internal Timer Clock domain run/stop signal. Clock sync delays apply before the value appears in the RUN SFR bit.
4. The uncertainty of the output is due to the prescaler setting.
5. Timer Out (Level) rises along with ERS when START = Rising/Either ERS Edge.
6. Timer Out (Level) falls synchronous to the timer clock.
7. Cleared by software.