BANK 61

1E80h 1E8Bh	Core registers
1E8Ch	ANSELA
1E8Dh	WPUA
1E8Eh	ODCONA
1E8Fh	SLRCONA
1E90h	INLVLA
1E91h	IOCAP
1E92h	IOCAN
1E93h	IOCAF
1E94h	—
1E95h	—
1E96h	ANSELB
1E97h	WPUB
1E98h	ODCONB
1E99h	SLRCONB
1E9Ah	INLVLB
1E9Bh	IOCBP
1E9Ch	IOCBN
1E9Dh	IOCBF
1E9Eh	—
1E9Fh	—
1EA0h	ANSELC
1EA1h	WPUC
1EA2h	ODCONC
1EA3h	SLRCONC
1EA4h	INLVLC
1EA5h	IOCCP
1EA6h	IOCCN
1EA7h	IOCCF
1EA8h	—
1EA9h	—

1EAAh	ANSELD(1)
1EABh	WPUD(1)
1EACh	ODCOND(1)
1EADh	SLRCOND(1)
1EAEh	INLVLD(1)
1EAFh 1EB3h	Unimplemented Read as '0'
1EB4h	ANSELE(1)
1EB5h	WPUE
1EB6h	ODCONE(1)
1EB7h	SLRCONE(1)
1EB8h	INLVLE
1EB9h	IOCEP
1EBAh	IOCEN
1EBBh	IOCEF
1EBCh 1EE2h	Unimplemented Read as '0'
1EE3h	RB1I2C
1EE4h	RB2I2C
1EE5h 1EEAh	Unimplemented Read as '0'
1EEBh	RC3I2C
1EECh	RC4I2C
1EEDh	—
1EEEh	RD0I2C(1)
1EEFh	RD1I2C(1)
1EF0h 1EFFh	Common RAM (Accesses 70h-7Fh)

Note: 1. 40-pin devices only.

Legend:

Unimplemented data memory locations, read as '0'